Pipeline ADC

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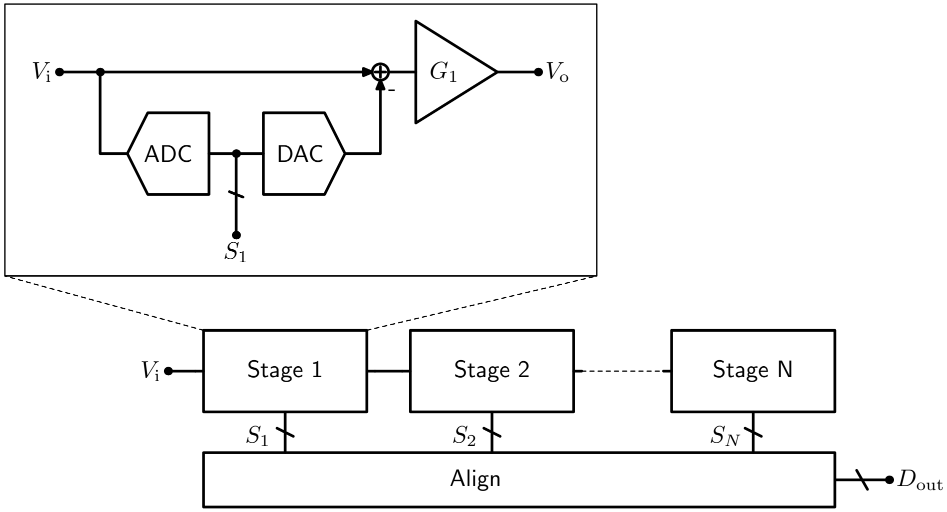
Abstract

A quick introduction.

Pipeline ADC: Gain of 4, 6/8 latch pipeline



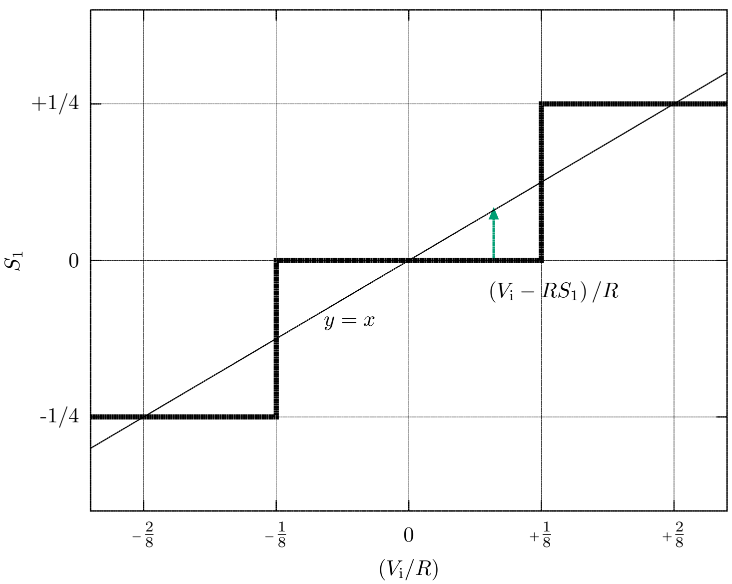
$$V_o = G_1 \cdot (V_i - R \cdot S_1)\,, \quad G_1 = 4$$

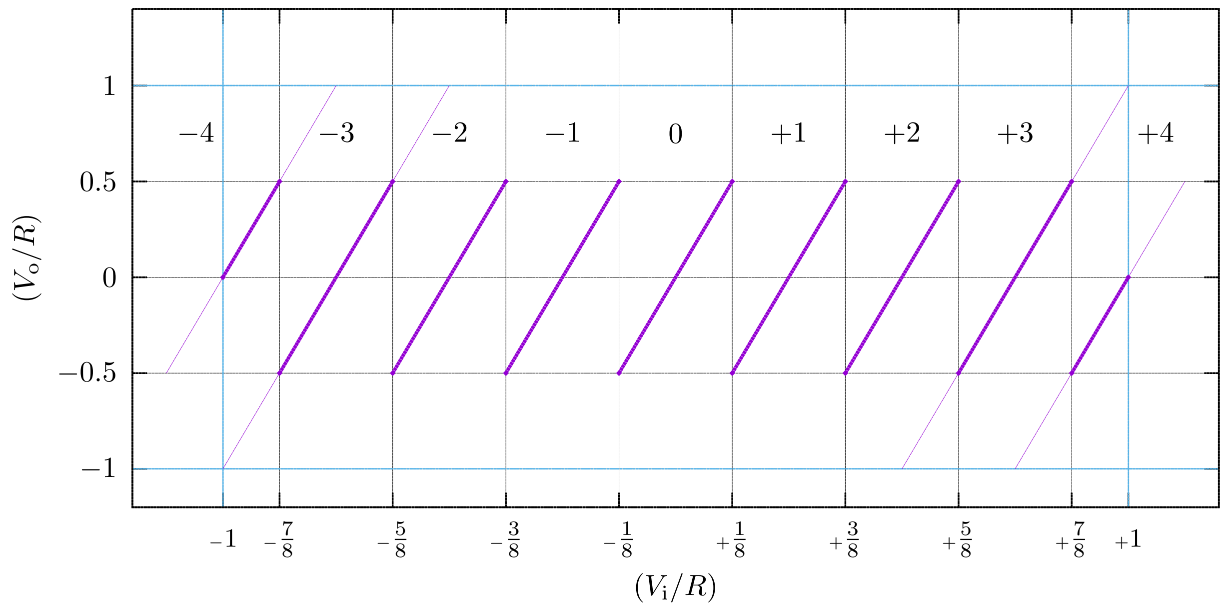
$S_1 = \{-1, -3/4, \ldots, +3/4, +1\}$ (Fixed point real)

R : Reference voltage

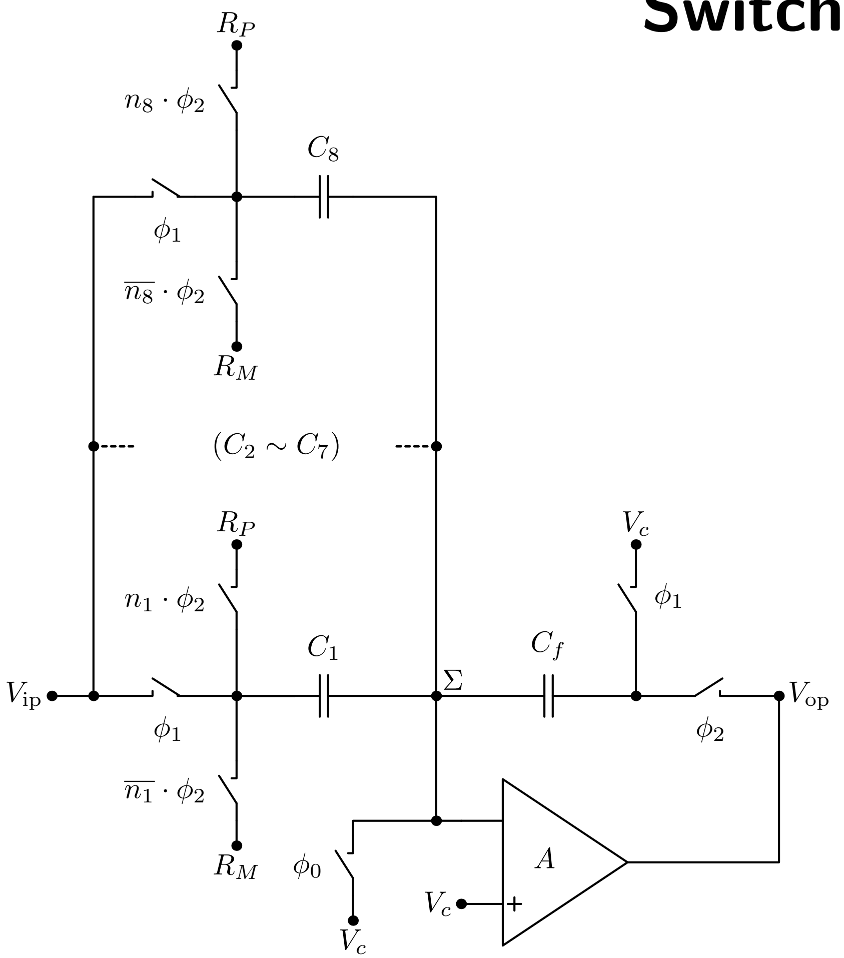
$$\left(\frac{V_i}{R}\right) = S_1 + \frac{1}{G_1} \cdot \left(\frac{V_o}{R}\right).$$

V_o is "residue", quantization error of SubADC.





Switched Cap MDAC



$$C_f = 2C_j, \quad j : 1 \sim 8$$

$$n_j = -1 \;\text{ or }\; +1$$

$$G = 8\,C_j/C_f = 4$$

$$V_{\rm i} = V_{\rm ip} - V_{\rm im}$$

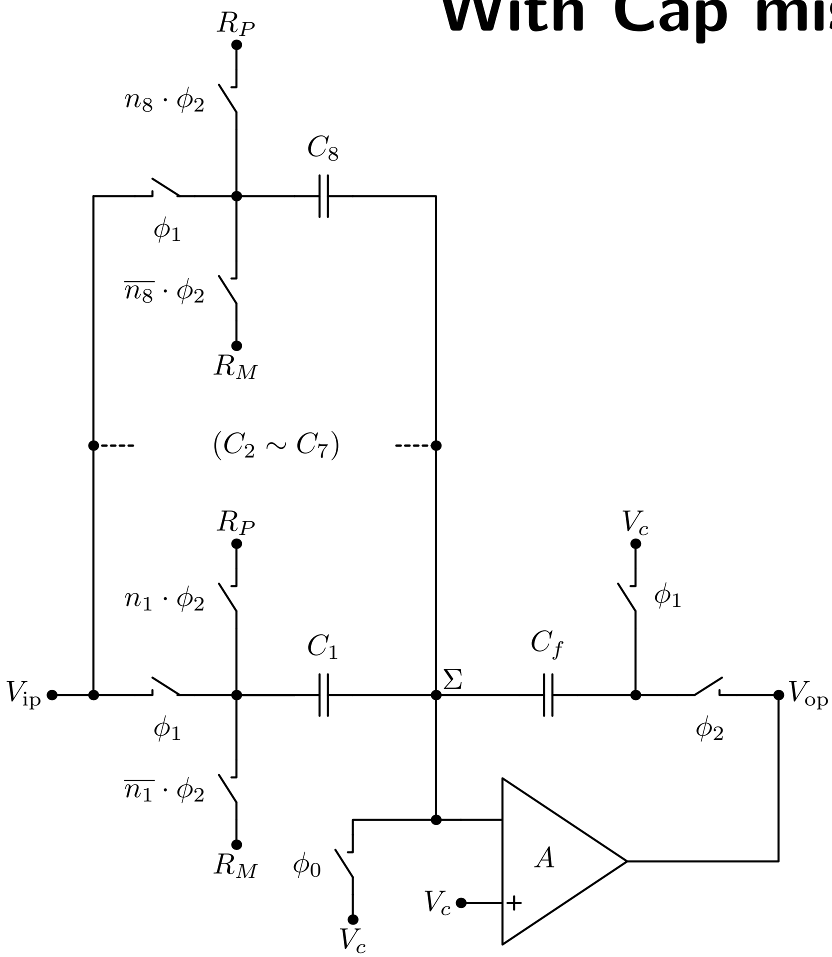
$$V_{\rm o} = V_{\rm op} - V_{\rm om}$$

$$R = R_P - R_M$$

$$\left(\frac{V_{\rm i}}{R}\right) = \frac{\sum n_j}{8} + \frac{1}{4} \cdot \left(\frac{V_{\rm o}}{R}\right)$$

- n_j: $\{+1, -1\}$. Thermometer output of SubADC Quant.
- (V_o/R) is ranging from -1 to +1, can be replaced by backend ADC's output.
- Mismatch in C_j shows up as offset associated with code j. Resulting non-linearity. (next page)
- Mismatch between C_f and $\sum C_j$ shows up as gain error. (next page)
- κ : amplifier's gain error. κ' : overall gain error including next stage's gain error. (next page)

With Cap mismatch and gain error



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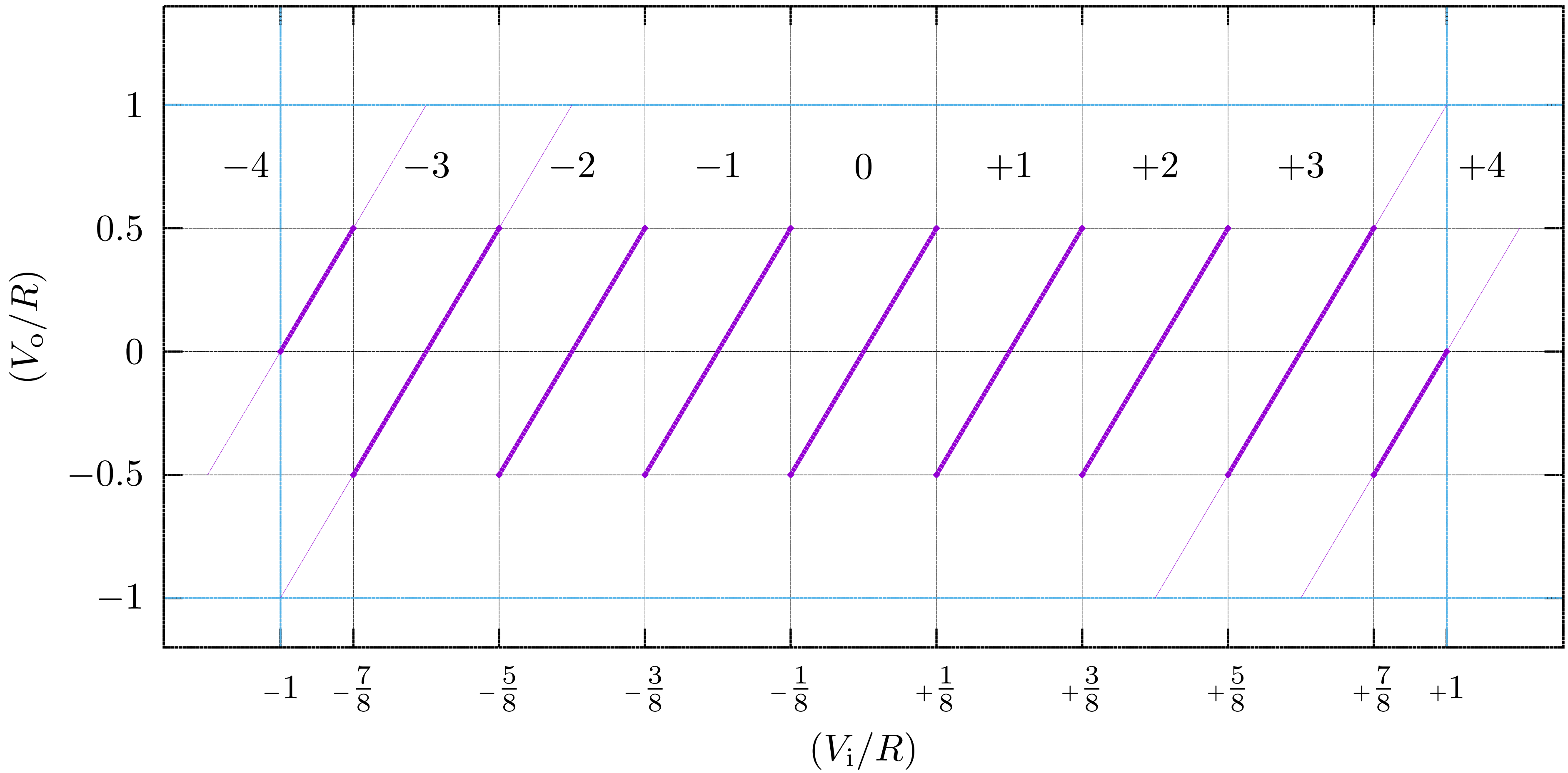
$$\left(\frac{V_{\rm i}}{R}\right) = \frac{\sum n_j}{8} + \frac{1}{4} \cdot \left(\frac{V_{\rm o}}{R}\right)$$

With $C_j = (C_f/2)\,(1 + \delta_j)$ and gain error factor κ',

$$\sum_j \frac{(1+\delta_j)}{8} \left(\frac{V_{\rm i}}{R}\right) = \frac{\sum n_j}{8} + \frac{\kappa'}{4} \left(\frac{V_{\rm o}}{R}\right) + \frac{\sum n_j \delta_j}{8}$$

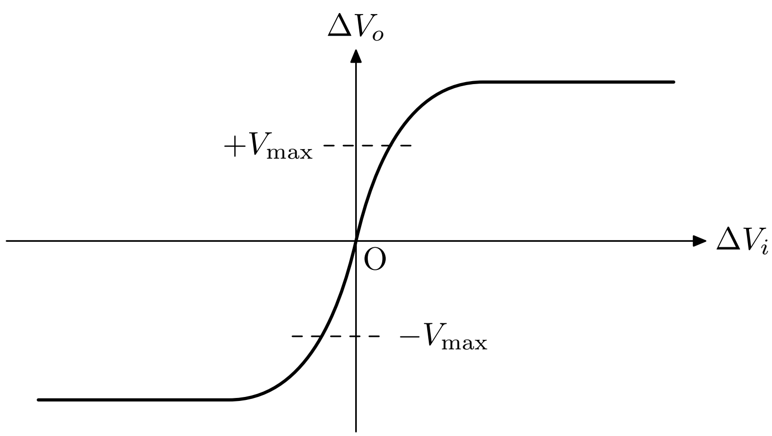
Transfer function and Source of NL

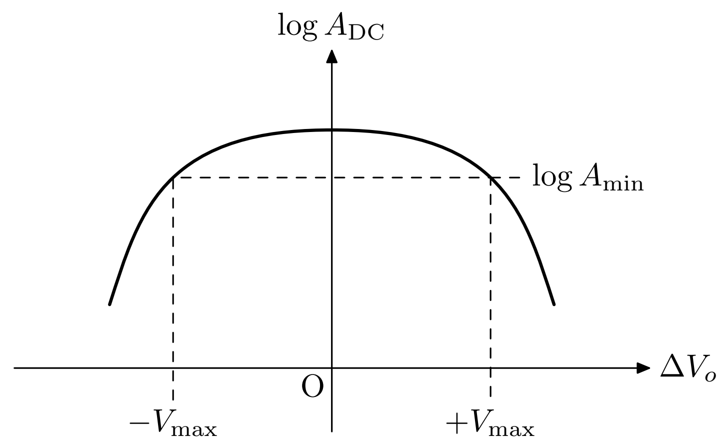


- Gain error (κ') affects the slope of each segment.
- Capacitor mismatch (δ_j)shows up as offset of each segment.
- SubADC's error will enlarge output swing. But does not affect overall linearity directly.

Things we cannot trim

One of the reason why we cannot trim perfectly is opamp's insufficient linearity range.

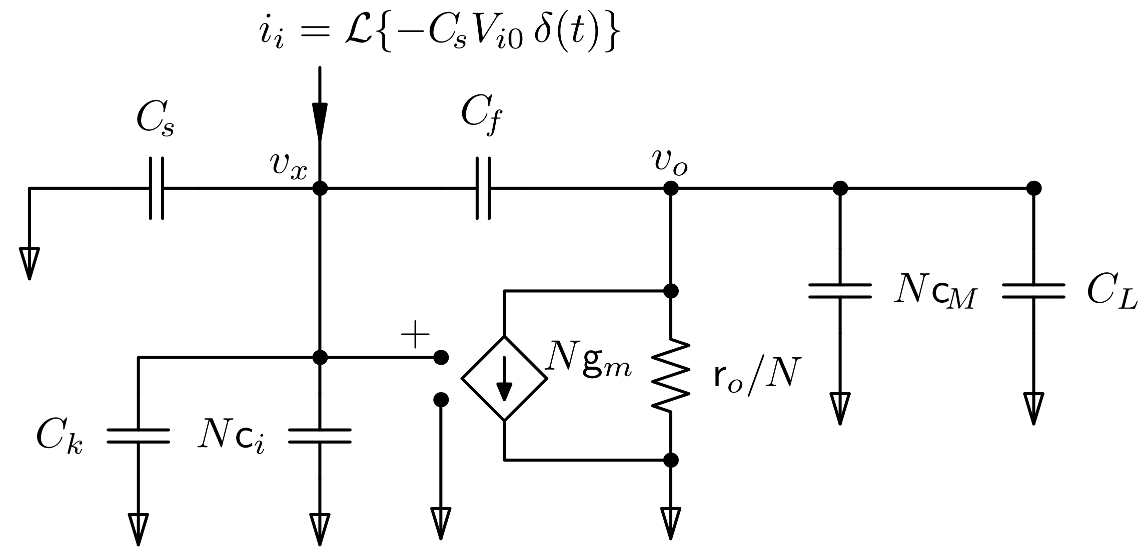




Speed and linearity trade off is where opamp designer spend most of time.

Amplifier Scaling

Adjust “width” of the amplifier, N.



$g_m = N\mathsf{g}_m$,

$R_o = \mathsf{r}_o/N$,

$C_i = N\mathsf{c}_i$,

$C_M = N\mathsf{c}_M$,

$\tau_A =$ Unity gain specific time.

$G_\tau =$ Inverse of feedback factor.

Settling time constant: $\tau = \tau_A G_\tau$,

$$\tau_A = \left(C_f(1 - 1/G_\tau) + C_M + C_L\right)/g_m, \quad G_\tau = (C_f + C_s + C_i + C_k)/C_f.$$

- There is an optimum N which makes τ minimum. (See G_τ)
- One goal is to make c_M as small as possible (find zero CM offset condition).

Amplifier Noise

Noise spectral density of input pair.

$$\langle v_{N_i}^2 \rangle_\omega d\omega \;=\; \frac{4k\Theta}{g_{m_i}} \cdot K_{th} \cdot \frac{d\omega}{2\pi} \;+\; \frac{k\Theta}{C_g} \cdot K_f \cdot \frac{d\omega}{\omega},$$

Input referred ($G = C_s/C_f$) noise (thermal only):

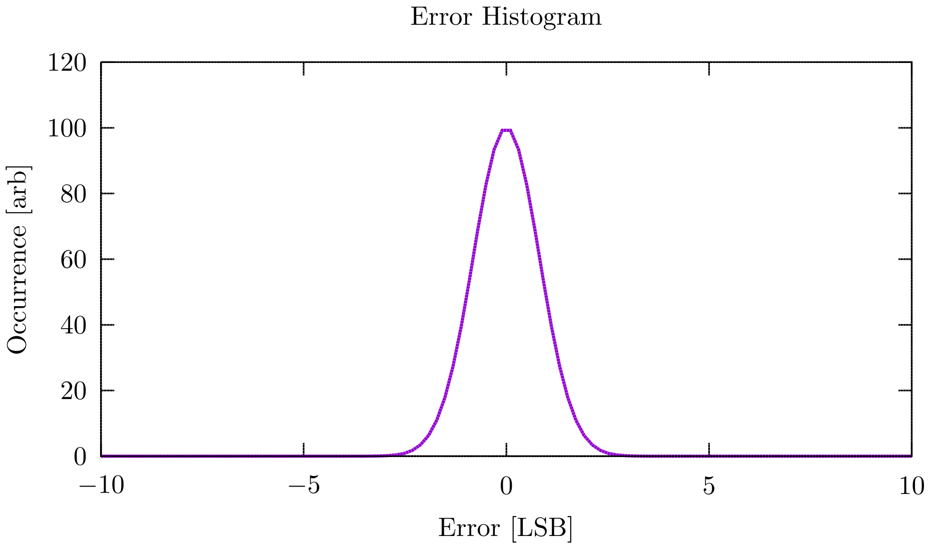
$$\frac{1}{G^2} \int_0^\infty \langle v_o^2 \rangle_\omega d\omega \;=\; \frac{k\Theta}{C_s} \cdot \frac{C_f}{C_L} \cdot \frac{G_\tau}{G} \cdot K_{th},$$

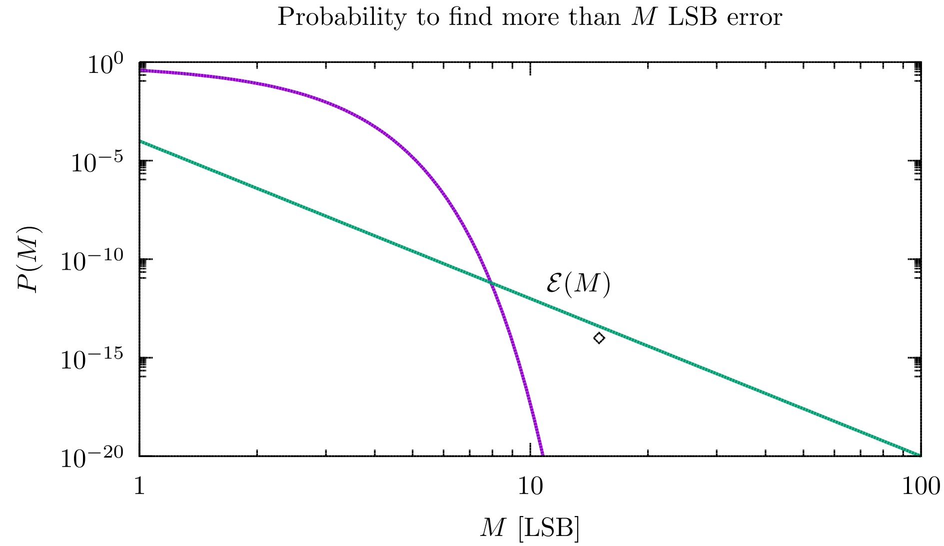
High gain setting gives better noise factor. ($C_f/C_L \sim 1$)

Total noise power is sum of

- Sampling (track mode) noise ($k\Theta/C_s$)
- Amplifier (hold mode) noise (second stage's sampling noise)
- Reference noise (S_1 dependent, does not contribute to idle channel noise)
- Flicker's contribution is proportional to $\ln T_s/\tau_A$ (??)

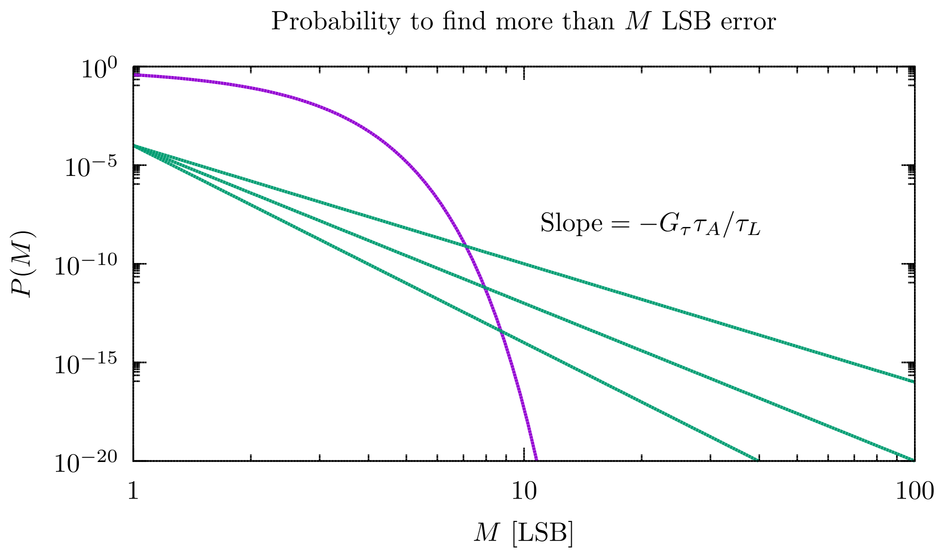
Error Rate

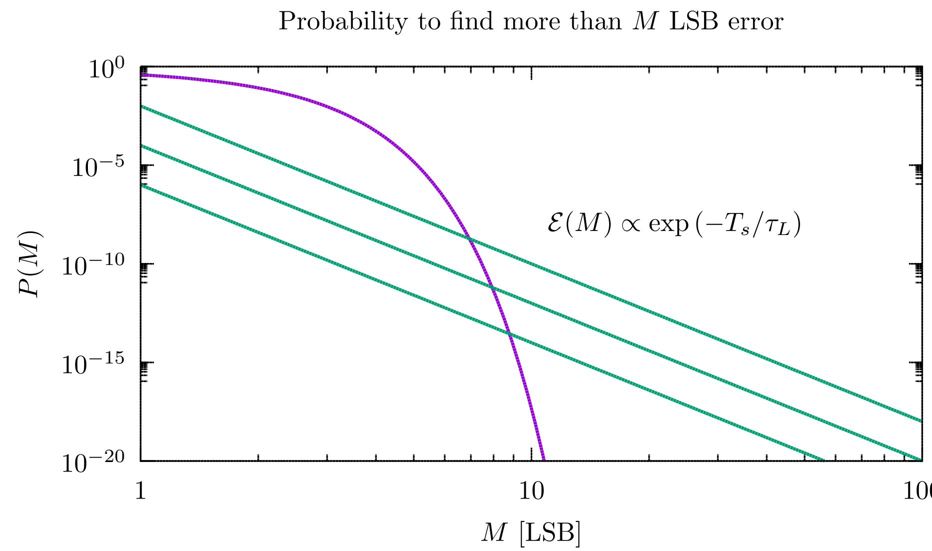




- Ideally, we would expect thermal noise only, which has gaussian distribution.
- Error rate, $P(M)$ is probability to find greater than M LSB error.
- Sometimes, usually at high sample rate, we find large error more often than we would expect from gaussian. (Sparkle error)
- That's the error caused by latch metastability: $\mathcal{E}(M)$.

Error Rate (Pipeline)





$$\mathcal{E}(M) \quad \propto \quad M^{-G_\tau \tau_A \,/\, \tau_L} \qquad\qquad \mathcal{E}(T_s) \quad \propto \quad e^{-T_s/\tau_L}$$

- Well optimized $G = 2$ pipeline is prone to high error rate.
- $\mathcal{E}(T_s)$ is very sensitive to τ_L... or T_s.
- For 30ps settling, τ_L of 7ps would give $\mathcal{E} \gtrsim 10^{-9}$ at 1.33Gsps.
- You can calculate τ_L from $\mathcal{E}$ vs T_s plot.

Number of Latch Operation

How many decisions do we need for 7bit ADC?

Flash: 127

G of 8, 34 pipeline: $16 + 15 = 31$

G of 4, 223 pipeline: $8 + 6 + 7 = 21$

G of 2, 111112 pipeline: $4 + 2 + 2 + 2 + 2 + 3 = 15$

SAR: 7

Challenges

- Amplifier: Make input cap as small as possible. Swing vs J_d
- Sampling: Align ϕ_0 between Quant and MDAC or SHA (inefficient)
- Refamp: Q transfer: C_sV (pipeline), $C_{\mathsf{par}}V$ (SAR)